ELECTRO-THERMAL SIMULATION OF A SEMICONDUCTOR DEVICE BASED ON SIMULATIVELY EXTRACTED ELECTRICAL PARAMETERS FROM MEASUREMENTS

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Abstract

In order to investigate degradation phenomena in the metallization of power semiconductor devices, a test chip with integrated N-type poly-silicon heaters has been designed. The goal is to correlate degradation rate with the temperature rise. To obtain the temperature rise electro-thermal FEM simulations were performed. The test chip has not been produced using standard semiconductor processes. Therefore a combination of measurements and FEM simulations has been applied to determine the temperature dependent electrical resistivity of the poly-silicon. Based on the measurements of the total heaters' resistance, the electrical resistivity was determined by iterative way of minimizing error between measurements and simulations for each temperature point. As a result, the proper temperature dependent material model of the poly-silicon was obtained. By means of the physically meaningful equation, the poly-silicon model was extrapolated for higher temperatures. Subsequently, the test chip temperature in the reliability investigations could be determined. The simulations have shown very good correlation with the actual measurements.

Keywords: FEM, electro-thermal simulation, semiconductor, temperature dependence

Presenting Author's biography

Vladimír Košel, graduated in 2003 in electrical engineering at Slovak University of Technology (STU) in Bratislava, with focus on DSP and integrated optoelectronics. He received his PhD in 2009 from STU FEI. During his PhD study was working on reliability of power devices at Infineon Technologies Austria and at KAI GmbH. Nowadays, he is working as R&D engineer at KAI GmbH.

1 Introduction

Due to continuous dimensions shrinking of smart power DMOS (Double Diffusion MOS) transistors, the energy density dissipated in the device during short-circuit or unclamped inductive switching events increases [1, 2, 3]. Repetitive operation under such conditions causes a gradual mechanical degradation of metallization layers [5, 6] which can lead to sudden destruction due to thermal runaway [4]. Additionally, the resulting mechanical fatigue of aluminum can cause cracking of the passivation layers [5, 7]. Therefore, it is very important to know the layer temperature in order to understand the degradation mechanisms and to improve metallization concepts. Special test structures with poly-silicon heaters emulating power transistors have been previously used for the study of degradation of power metal layers covered by hard (oxide) passivation layers [5, 7].

A similar test chip has been designed to investigate the degradation phenomena caused by the cyclic change of temperature. The test chip consists of silicon die and integrated poly-silicon heaters which have the form of very thin elongated rectangular plates. In the reliability investigations the heaters are loaded with periodic voltage pulses causing the current flow and subsequently temperature rise in the whole device. The final goal is to correlate the life-time or degradation rate with the temperature rise, gradients or generally with the 3D temperature distribution. To obtain the 3D temperature distribution, the electro-thermal FEM simulations were performed using ANSYS. Because the designed test chip had not been produced using standard semiconductor processes, it was necessary to determine the electrical resistivity of the poly-silicon. The poly-silicon has a thickness of 290 nm and is heavily doped with phosphor. It is well known that doped poly-silicon is a material whose electrical resistivity (conductivity) is significantly dependent on temperature. This fact made the investigation more difficult.

The temperature dependent electrical resistivity was determined by a combination of both the laboratory measurements and FEM simulations. Based on the measurements of the heaters' resistance, the electrical resistivity was determined by iterative way of minimizing error between measurements and simulations for each temperature. To automate this procedure the optimization features of APDL (ANSYS parametric design language) were used. As a result, the proper temperature dependent material model of the poly-silicon was obtained. Subsequently the test chip temperature in the reliability investigations was determined.

2 Test chip and its FEM model

2.1 Test chip description

Four test structures (heaters) are implemented on the layer stack consisting of N+ (highly doped) silicon substrate with N- (lowly doped) epitaxial layer covered with an oxide layer for electrical isolation. The heaters made of polycrystalline gate silicon are structured atop of the oxide layer (Fig. 1). The heaters substitute power transistors. The layers above the poly-silicon heaters may be built in with different layer compositions (different materials and thickness) within the limits of the technology fabrication process (Fig. 2a). The layer composition used in this investigation is depicted in Fig. 2b. The test chip is mounted in a ceramic package. The electrical connections between the chip and the package are created using thin gold bonding wires.

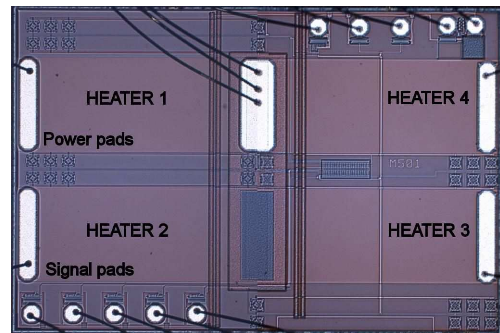
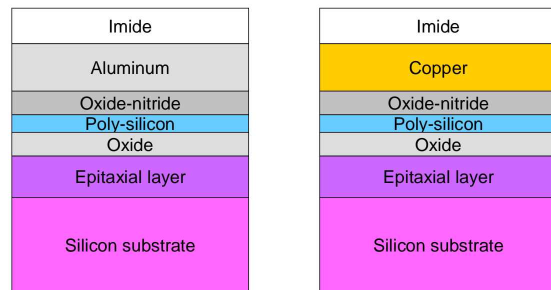


Fig. 1 Optical micrograph of the test chip

(a)



(b)

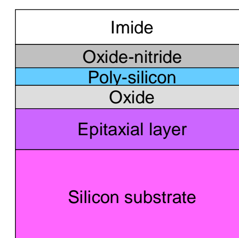


Fig. 2 Schematic cross-sections of the heater, a) examples of possible layer compositions, b) layer composition used in the investigation. Layer thickness varies from hundreds of nanometers up to hundreds of micrometers (not to scale)

2.2 Geometrical and FEM modeling

A 3D geometrical model of the test device has been created in the ANSYS Classic simulator (see Fig. 3 and Fig. 4). The emphasis was put on the exact modeling of upper part of the test chip. The model consists of six layers: silicon substrate, silicon epitaxial layer, silicon oxide, polycrystalline silicon, oxide-nitride and imide. The layer composition used is shown in Fig. 2b. The thickness of each particular layer has been determined using analytical methods such as FIB (Focused Ion Beam) sectioning. It is of high importance to know the exact layer thicknesses, as they can significantly influence electrical and thermal behavior of the model. The shape of the integrated structures in the XY plane is modeled upon the CAD data used for the test chip production. Simplifications are introduced for the arrangement of the gold bonding wires. The signal bonding wires connected to the small circular pads (see Fig. 1) are neglected as they have no influence on the heat removal from the heaters. The bonding wires connecting the large aluminum pad to the assigned lead in the package are replaced by a single wire. Due to the high electrical conductivity of gold and aluminum, these simplifications have negligible impact on the current and voltage distribution.

The electrical properties of the package leads, bonding wires and aluminum pads are assumed to have values of bulk materials. As already shown in the previous work [8], it is important to consider the temperature dependent thermal conductivity and specific heat capacity of silicon. The poly-silicon layer of the heaters is separately characterized as shown in the next section. All other thermal material parameters were assumed as temperature independent.

2.3 Determination of poly-silicon resistivity

In the first step, the temperature dependence of the total resistance of the heater was determined. The following approach has been applied. The temperature of the test chip was controlled by airstream (a laboratory equipment blowing air locally with predefine speed and temperature). The temperature dependent electrical resistance of the heater was obtained by four-point probe method in the range from -40°C to 180°C (see Fig. 5). This temperature range covers approximately the ambient temperature of smart power devices in the real application and is the maximum operating range of the airstream as well. However, power devices subjected to extreme conditions may be exposed internally to thermal stress exceeding 250 °C [9]. Thus, it is necessary to find an extrapolation function for higher temperatures.

Knowing the exact geometry of the heater shown in Fig. 1, it is possible to calculate the electrical resistivity of the poly-silicon. Due to the complexity of the heater form and electrical contacting from the top it is not possible to use analytical formulas.

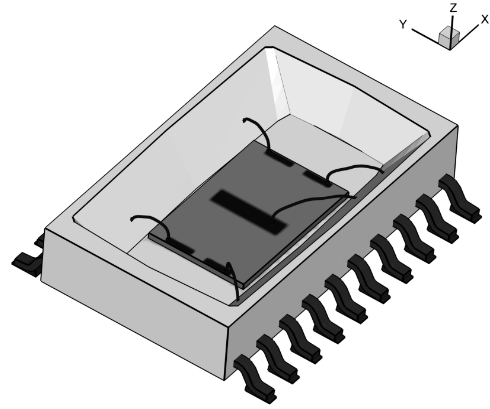


Fig. 3 3D geometrical model of the test chip created in ANSYS Classic

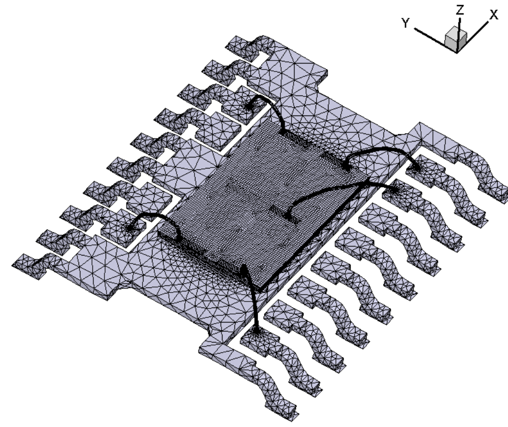


Fig. 4 3D FEM model of the test chip created in ANSYS Classic. Molding compound not shown

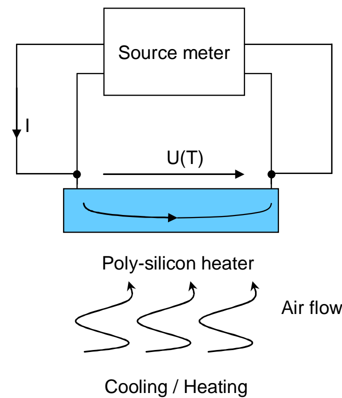


Fig. 5 Measurement setup for determination of the temperature dependent electrical resistance of the heaters

Therefore FEM method was used instead. An APDL code was written to determine resistivity from the measured resistance of the heater. The APDL code repeated the electro-thermal simulation and changed electrical resistivity until the maximum error allowed was reached, namely n-times for each temperature step respectively. The flow diagram of this procedure is shown in Fig. 6.

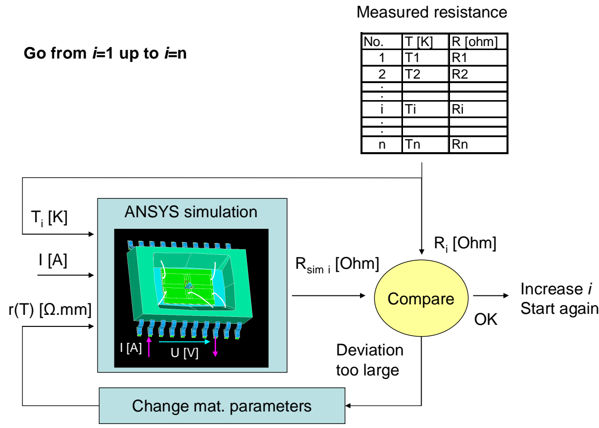


Fig. 6 Flow diagram - simulative determination of temperature dependent resistivity of poly-silicon

In the next step, the simulatively determined resistivity was fitted with the following equation:

$$\rho(T) = \rho_0 \cdot \left[1 + \left(\frac{T}{T_0}\right)^c\right] \quad (1)$$

where ρ [Ωmm] is the specific electric resistivity, T [K] is the temperature. The resistivity increase with temperature is caused by the decreasing mobility of the free carriers. This equation has a physical meaning and according to the theory of semiconductors can be used as a good approximation in the temperature range considered. The fitting parameters are determined from measurement data as follows:

ρ_0 = 4.98E-4 Ω.mm, T_0 = 138.78 K and c = 1.52.

Based on the fitting Eq. (1), the electrical resistivity was extrapolated up to 600 K (solid line in Fig. 7).

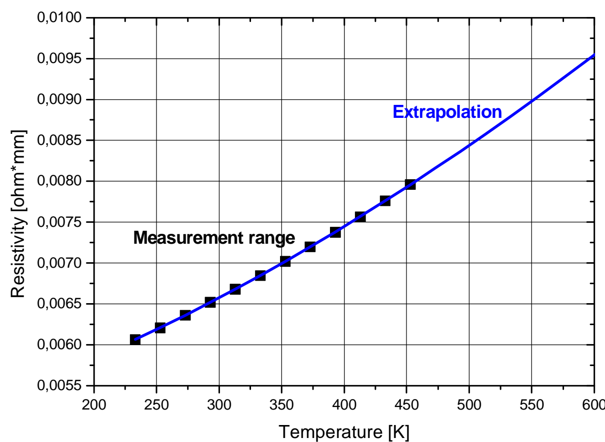


Fig. 7 Temperature dependency of electrical resistivity ρ of the used poly-silicon (square symbols are measurements; solid line stands for fitting)

Further, it was possible to estimate the doping concentration in the heater out of the determined resistivity. In [10] a plot showing dependency of electrical resistivity on doping concentration and type of doping atoms has been published. Our poly-silicon has at room temperature a resistivity value of about 0.65 mΩ.cm which corresponds to a doping concentration of about 3.5×10^{20} cm^{-3}.

3 Test chip subjected to a stress pulse

Transient measurements were performed to evaluate the temperature in the test chip while stressed by a short power pulse (pulse length = 2.2 ms, amplitude = 71 V). Additionally, the simulation was used to verify the poly-silicon material model and modeling considerations.

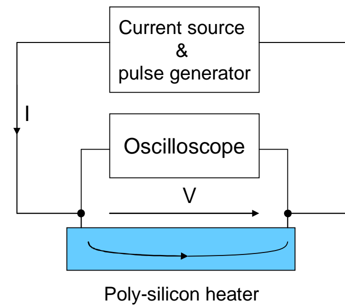


Fig. 8 Measurement setup of transient events

The measurement setup is shown in Fig. 8. The heater was fed with a current from a current source controlled by a pulse generator. The current and the voltage across the heater were recorded by an oscilloscope. In Fig. 9, the red solid line stands for the current of the stress pulse. The black thin line stands for the voltage across the heater. The decrease of the current from ~1.2 A down to ~1.1 A during the stress pulse is caused by the positive temperature coefficient of the heater's resistance. The measured electrical resistance at the end of the stress pulse corresponds to a mean temperature of 152 °C. As shown later this value is much lower than the maximum temperature. In order to get more information on temperature distribution, electro-thermal FEM simulations were performed. The recorded voltage waveform was used as electrical boundary condition in the simulation. The result of the simulation is the current flowing through the heater, electrical potential and temperature distribution. A good assessment of the simulation accuracy can be obtained by comparison between the measured and simulated current waveform. Both can be seen in Fig. 9. The waveforms fit each other very well.

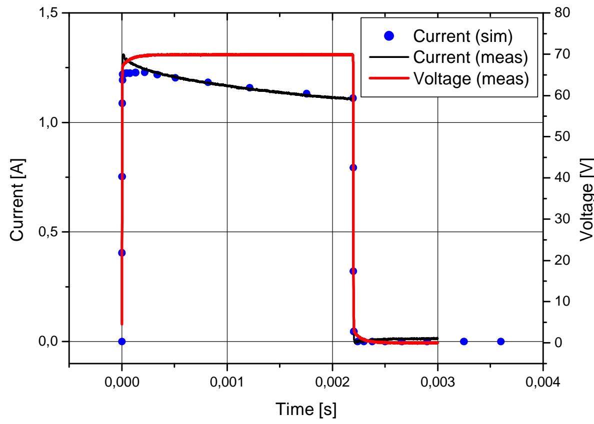


Fig. 9 Thick solid line: voltage measured, Thin solid line: current measured. Circuit symbols: the current calculated using electro-thermal FEM simulation

Fig. 10 shows the temperature distribution in the poly-silicon layer acquired through the electro-thermal FEM simulation. The temperature distributions in the heater region along the central line A-A as defined in the 2D temperature image (Fig. 10) are shown in Fig. 11. The curves shown in Fig. 11 describe the temperature distribution in different layers (imide, poly-silicon). A maximum temperature of about 180 °C was observed. Great temperature differences can be seen between particular layers. Such information is important for life-time analysis of power devices.

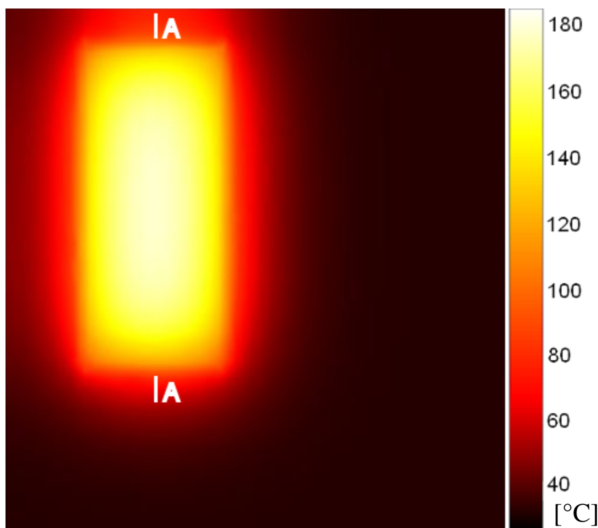


Fig. 10 Temperature distribution in the test chip at the height level of the poly-silicon (see also Fig. 2)

Fig. 12 shows the maximum temperature development in different layers. The time delay between the curves is caused by the thermal dynamics of the layers which is related to the absolute values of the specific heat capacity and thermal resistivity. In principle this delay is proportional to the heat transfer time from the poly-silicon layer to the test chip surface and vice-versa. At the end of the applied pulse, the surface temperature is about 7 °C lower than the temperature in the heater. During the cooling phase the difference is even larger. Interesting phenomena can be seen during the cooling phase. The heat is removed faster from the heater than from the chip surface. This is caused by the high thermal resistance of imide and air.

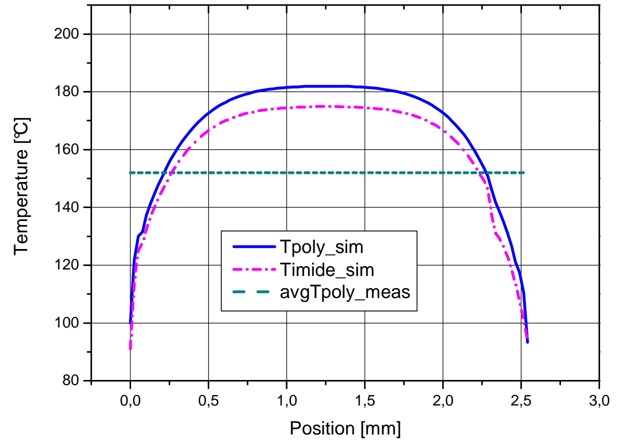


Fig. 11 Temperature distributions along the line cut A–A (see Fig. 10) of the active region. Solid line: poly-silicon surface. Short dash-dotted line: imide surface. Straight dashed line: Mean temperature of the poly-silicon layer (based on the heater resistance)

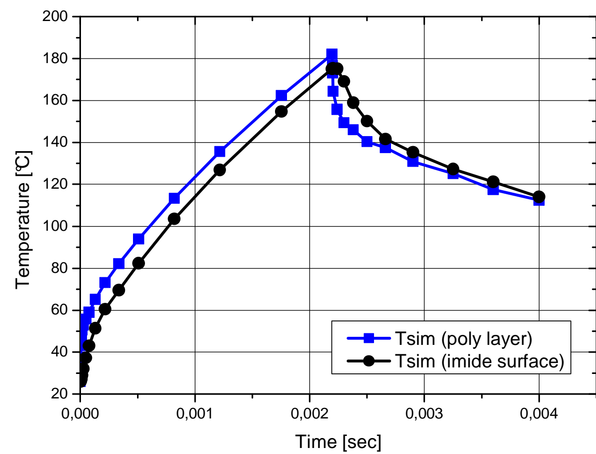


Fig. 12 Maximum temperature on the poly-silicon (squares) and imide surface (circles) vs. time

4 Conclusion

A test chip for investigations of degradation phenomena in metallization has been designed. Using this test chip it is possible to generate temperature rise similar to that occurring in power transistors subjected to extreme electrical conditions. In comparison to the

power transistors, such poly-silicon heaters allow us to investigate degradation phenomena under very broad operating conditions and for different composite layers.

Using a simulation approach, electrical resistivity of the poly-silicon material was determined with good accuracy over a broad temperature range. Furthermore, the resistivity was extrapolated for higher temperatures by means of a physically meaningful equation. Application of this material model to electro-thermal simulations of transient events has shown a very good correlation with the actual measurements. In addition, it was observed that in such fast transient thermal events the temperature rise is concentrated in the heater and its very close vicinity. The temperature, particularly in thin layers can significantly differ in both time and space. This has to be taken into account at the analyses of life-time tests.

5 Acknowledgement

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